**INTRODUCTION:**

* Detailed routing is a critical stage in VLSI physical design. The interconnections including wires and vias need to be constructed satisfying various design rules.
* Facing the high complexity of the detailed routing problem, there are two main approaches to solve it, including sequential approach and concurrent approach.
* Sequential approach uses iterative rip-up and reroute (R&R) to reduce the number of design rule violations (DRVs) [1]–[7].
* The concurrent routing approach formulates detailed routing as integer linear programming (ILP), Boolean satisfiability(SAT), or satisfiability modulo theories (SMT) problems [9]–[11]. In this approach, route construction of multiple nets are performed concurrently to optimize the solution quality.

A well-studied formulation is to treat the assignment of each routing grid point to a net as a decision variable, and model connectivity and design rules as constraints. It generates high quality solutions, but often requires long runtime. As a result, it is generally applied in small routing regions (e.g., 10 tracks *×* 10 tracks).

As studied in FPGA detailed routing [12], another formulation is to use

choices in possible net routes as decision variables. It is more scalable than the routing-grid-based formulation